

# ANN Model of High Electric Field Stress in n-channel VDMOS Power Transistors

Aleksandar Vulović, Milan Savić, Sanja Aleksić, and Dragan Pantić

**Abstract** - One of the most common causes of unstable operation of power VDMOS transistor is the exposing of the gate oxide to high electric field, which happens when the voltages, whose the values are similar to the breakdown voltage, are conducted onto the gate contact. Processes that are occurring in the oxide and semiconductor bulk and at the Si/SiO<sub>2</sub> interface are very complex and it is therefore impossible to create an acceptable and accurate physical model to describe the device characteristics. In this paper, we have applied artificial neural networks (ANN) for modeling and simulation of high electric field stress (HEFS) in n-channel VDMOS power transistor. To build ANN HEFS-nVDMOS model we used measured transfer characteristics  $I_D=f(V_{GS})$ , for different times of stress. Different neural network structures were tested and optimized to obtain the best ANN HEFS-nVDMOS model configuration<sup>1</sup>.

**Keywords** – neural network, n-channel VDMOS, simulation, model, high electric field stress.

## I. INTRODUCTION

There are problems in electronics that are very complex so it is almost impossible to define the corresponding unique physical model to describe these phenomena. That is why we will have to neglect some effects in the process of generating models, and therefore we have taken into account when to apply the appropriate model. On the other hand, even if we could generate a physical model of satisfactory accuracy, it would be so complex and practically inapplicable in TCAD software tools for process, device and circuit simulation. Effective solution, which imposes in cases like this, is the application of models which are generated by using the artificial neural networks (ANN). In contrast to traditional models, which are *theory-rich* and *data-poor*, ANN models are generated in a way that a little or no a priori knowledge of the problem is required [1-3].

ANN model design process consists of seven basic steps (Fig. 1) [4]. The first step is data collection. This procedure is realized independently of software tools which are used to generate the ANN model, but this step is critical to the success of the design process. Therefore, it is very important to carefully design and realize the experiment that will provide us with the necessary number of required

data. After a neural network has been created, which means to arrange the network to be compatible with our problem that we want to solve (step 2), it needs to be configured (step 3). After that the adjustable parameters of neural network (weights and biases) are first initialized (step 4) and their values are optimized and carefully tuned. This process is called neural network setup or training (step 5). Finally, we have the process of validation of the generated ANN model (step 6) and its use (step 7), if all tests have been successfully verified.

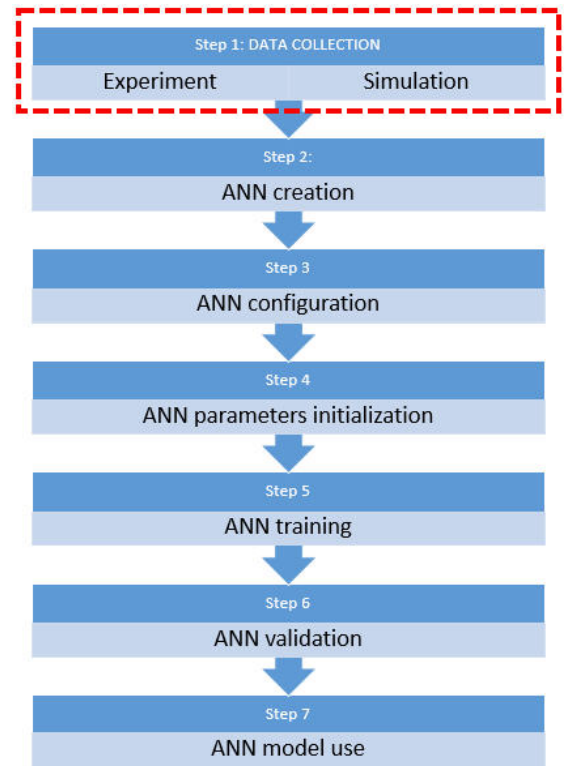


Fig. 1. The work flow for ANN model design [4].

When the high voltage, close to the breakdown voltage, acts on the gate contact, the instability of the VDMOSFET electrical characteristics occurs [5-9]. The charges which are generated in the gate oxide and at the Si/SiO<sub>2</sub> interface dominantly influence on the threshold voltage of VDMOS transistor. Processes that are occurring in the oxide and semiconductor bulk and at the Si/SiO<sub>2</sub> interface are very complex and it is therefore impossible to create an acceptable and accurate physical model to describe the device characteristics. In this paper, we will apply ANN for modeling of high electric field stress (HEFS) in n-channel

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VDMOS power transistor. To build ANN HEFS-nVDMOS model we will use measured transfer characteristics  $I_D=f(V_{GS})$ , for different times of stress in the range from 0 to 150 minutes. Different neural network structures will be test and optimize in order to obtain the best ANN HEFS-nVDMOS model configuration.

## II. NEURAL NETWORK MODEL DESIGN

### A. Data collection

Once a research problem has been determined the next step is to identify which method will be appropriate and effective for data collection. In our case there are two sources of data necessary for ANN model design. Primary data collection uses experimental results. The commercial n-channel VDMOS power transistor IRF510 [10] has been exposed to HEFS by  $V_S=80V$  on the gate contact for up to  $t_S=150$  minutes (Fig.2). The transfer characteristics  $I_D=f(V_{GS})$  is measured at defined time intervals at room temperature ( $T=25^\circ C$ ).

The secondary data source can be the results obtained by simulating the electrical characteristics of n-channel VDMOS power transistor under the influence of HEFS.

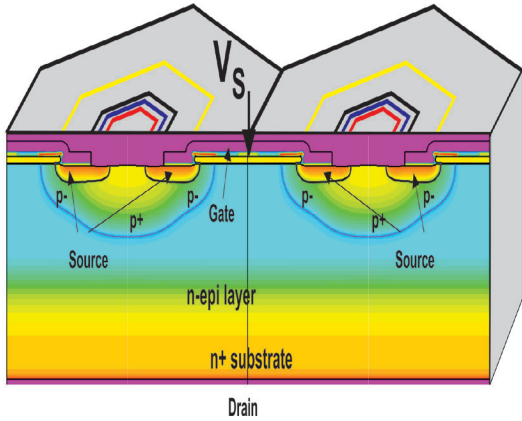


Fig. 2. The cross section of n-channel VDMOS power transistor.

### B. ANN creation and configuration

ANN model creation assumes that neural network corresponds to the problem we want to solve. In this case, we want to form a model that will be able to give us the transfer characteristics  $I_D=f(V_{GS})$  of n-channel VDMOS power transistor IRF510 which is exposed to HEFS. According to that, the input parameters of ANN HEFS-nVDMOS model are: stress voltage  $V_S$ , time of stress  $t_S$  and gate voltage  $V_{GS}$ , while the output parameter is drain current  $I_D$ . The block diagram of the proposed ANN HEFS-nVDMOS model is given in Fig. 3. Hence, our ANN model has 3 neurons in input layer (IL) and 1 neuron in output layer (OL). The structure and number of neurons in hidden layers (H1, H2) will be optimized in order to obtain the best ANN model accuracy.

Within the neural network configuration the definition of the connections between components of the network is

required. In our model there is a bias connected to each layer, inputs are connected to H1 and output comes from H2. Layers H1 and H2 are also connected. After a neural network has been created, it must be configured. It is necessary to define example data set of inputs and targets (desired ANN model outputs). It is very important to know that ANN model can only be as accurate as the data that are used to train the neural network. The defined sample data must first be processed. We need the minimum and maximum values of the defined data to perform the correct normalization so that all inputs fall in the range  $[-1,1]$  or  $[0,1]$ .

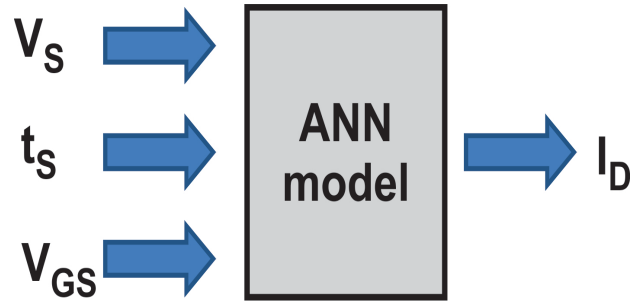


Fig. 3. The proposed ANN HEFS-nVDMOS model.

### C. ANN training and validation

ANN training can be more efficient if preprocessing steps on the sample data are performed. Typically, the normalization is applied to both the input and target data set. In that case, when ANN model is put to use output results fall into a normalized range and it is necessary to transformed it back into the units of the original target data. It is important that the data cover the range of inputs for which ANN model will be used. The data are first divide into three subsets: training set, validation set and test set. Training set is used for computing, tuning and updating the network weights and biases. Finally, after the initialization of the network weights and biases the ANN is ready for training.

The training process of ANN implies tuning the values of the weights and biases in order to optimize neural network performance and minimize sum square error (SSE). SSE is defined as sum squared error between ANN model outputs and target outputs. In our model we use Levenberg-Marquardt and Bayesian training algorithm. In hidden layers tan-sigmoid transfer function is used, while neurons in output layer have linear transfer function. ANN HEFS-nVDMOS model is tested with one and two hidden layers, while the number of neurons in these layers is changed from four to nine. Sum squared errors for different ANN model structures for train and test data sets are given in Table I. It is obvious that the best result is obtained for the network with two hidden layers with seven and nine neurons in H1 and H2, respectively. Schematic diagram of HEFS-nVDMOS neural network is shown in Fig. 4.

TABLE I  
SUM SQUARED ERROR (SSE) COMPARISON FOR DIFFERENT ANN  
STRUCTURE

ANN structure				SSE	
IL	H1	H2	OL	TRAIN	TEST
3	4	0	1	0.089931285	0.068499754
3	5	0	1	2.954554294	2.647080672
3	6	0	1	0.112300972	0.093437814
3	7	0	1	0.014032776	0.061402315
3	8	0	1	0.017724825	0.047014735
3	5	5	1	0.006783653	0.010740525
3	6	6	1	0.001738477	0.002346667
3	7	7	1	0.001709225	0.009891808
3	7	8	1	0.000926591	0.605611541
3	7	9	1	0.000325886	0.001180359
3	8	8	1	0.000230926	0.004370062

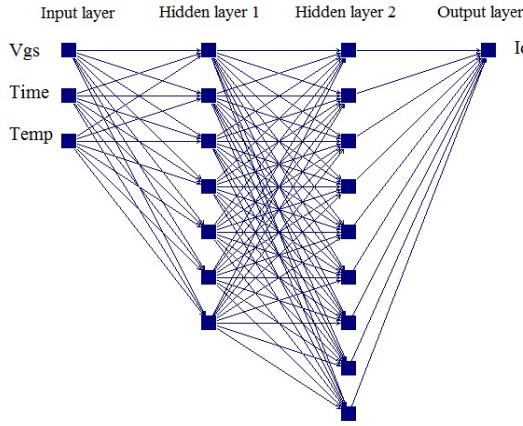


Fig. 4. Schematic diagram of HEFS-nVDMOS neural network.

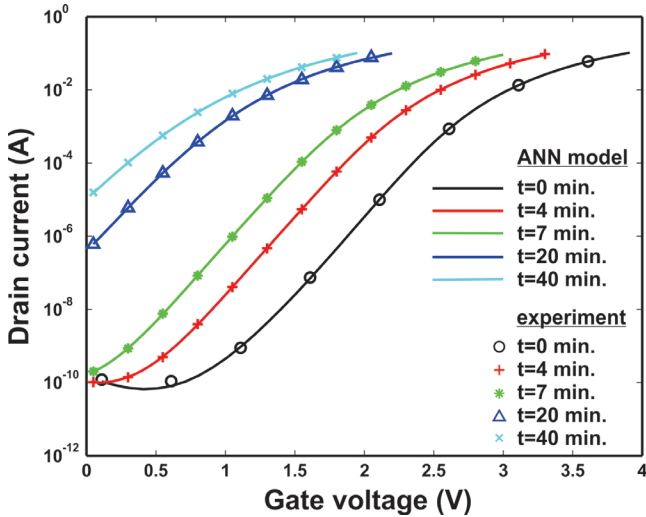


Fig. 5. Transfer characteristics  $I_D=f(V_{GS})$  of n-channel VDMOS power transistor IRF510 under HEFS with  $V_S=80V$ : ANN model (solid lines) and experiment (marks).

### III. RESULTS AND DISCUSSION

When the training of neural network is complete it is necessary to check its performance and determine if any changes need to be made. After the network is trained and validated, ANN model can be used to calculate the response to any input. In our case ANN HEFS-nVDMOS model gives the transfer characteristics  $I_D=f(V_{GS})$  of n-channel VDMOS power transistor IRF510 after the influence of  $V_S=80V$  on gate contact for an arbitrary time of stress  $t_s$  up to 150 minutes.

The comparison of transfer characteristics obtained with ANN HEFS-nVDMOS model with experimental results which were used for neural network training are shown in Fig. 5 and Fig. 6. A very good agreement is obtained, which is expected, considering the value of SSE which is given in Table I.

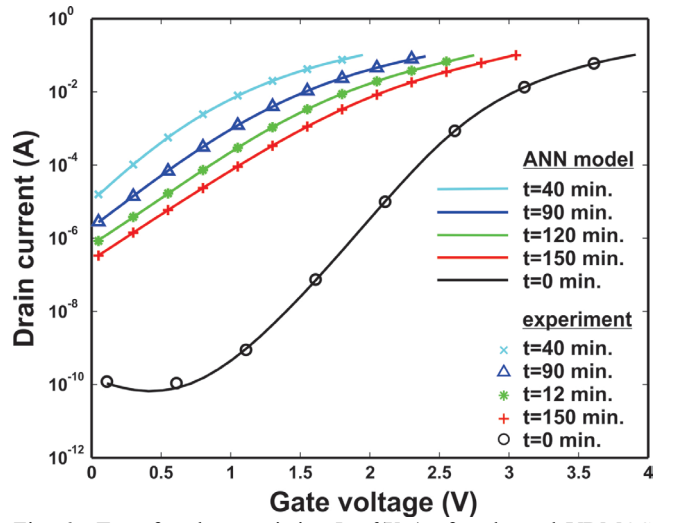


Fig. 6. Transfer characteristics  $I_D=f(V_{GS})$  of n-channel VDMOS power transistor IRF510 under HEFS with  $V_S=80V$ : ANN model (solid lines) and experiment (marks).

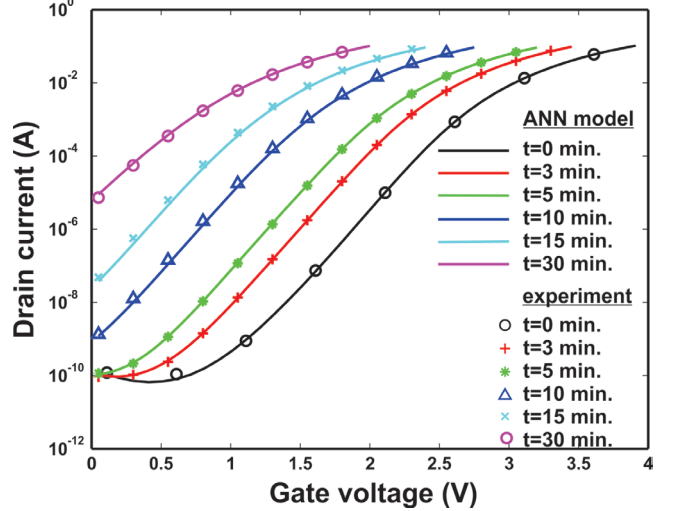


Fig. 7. Transfer characteristics  $I_D=f(V_{GS})$  of n-channel VDMOS power transistor IRF510 under HEFS with  $V_S=80V$ : ANN model (solid lines) and experiment (marks).

In Fig. 7 and Fig. 8 we made a comparison of transfer characteristics obtained with ANN model with the experimental results that have not been used in the process of neural network training. As in the previous case, very good agreement is obtained, which indicates that the neural network is well trained and that the generated ANN model can generalize well within the range inputs for which the network has been trained.

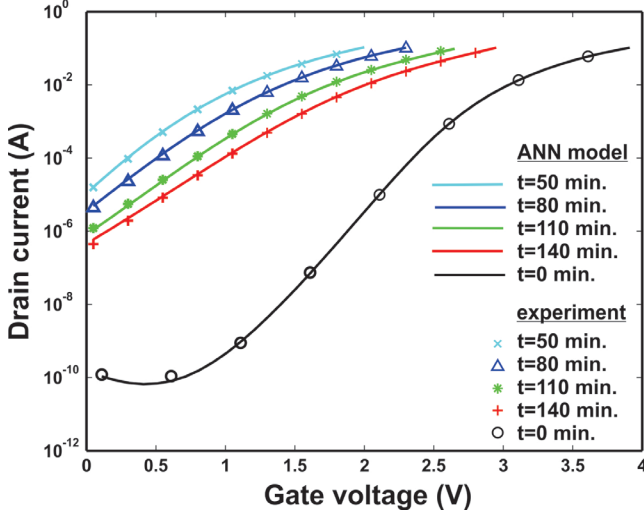


Fig. 8. Transfer characteristics  $I_D=f(V_{GS})$  of n-channel VDMOS power transistor IRF510 under HEFS with  $V_S=80V$ : ANN model (solid lines) and experiment (marks).

## V. CONCLUSION

In this paper, we have applied ANN for modeling of high electric field stress (HEFS) in n-channel VDMOS power transistor. To build ANN HEFS-nVDMOS model we used measured transfer characteristics  $I_D=f(V_{GS})$ , for different times of stress ( $t_s=0$  to 150 minutes). Different neural network structures were tested and optimized to obtain the best ANN model configuration (IL=3, H1=7, H2=9, OL=1) with a minimum SSE. The proposed ANN model gives very good agreement with the experimental results. This indicates on the great possibilities of the application of the models based on neural networks in this area.

## ACKNOWLEDGEMENT

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